REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 25-30,32,33 and 39 are pending in the application.

Claims 25-30,32,33 and 39 stand rejected.

Claim Rejections Under 35 USC § 102(b)

Claims 25-30,32,33 and 39 are rejected under 35 USC § 102(b) as being anticipated by Higashikawa et al '637. It is contended that Higashikawa discloses a lithographic semiconductor fabrication process including the steps of exposing a semiconductor wafer to a first mask that is at least partially defective to form a defectively exposed portion, then exposing the defectively exposed portion to a second mask part that is substantially free from defects or with defects at different locations for a second and a third time, to at least partially repair the defectively exposed portion on the wafer. The Examiner further contended that Higashikawa further discloses the first and second mask parts are formed on the same photomask, the first mask part and the second mask part are formed on different

photomasks, exposing the defectively exposed portion to a third mask part one or more times, exposing the defectively exposed portion to the second mask part a second and a third time, and exposing the defectively exposed portion to the second, a third and other additional mask parts one or more times.

The rejection of Claims 25-30,32,33 and 39 under 35 USC § 102(b) as being anticipated Higashikawa et al is respectfully traversed.

Higashikawa et al '637 discloses a method for repairing a defective portion of a photomask by:

1.**preventing exposure** (forming an unexposed portion) through the defective portion of a photomask,

2.forming an **opaque portion** over the defective portion prior to exposure, and then

3.exposing the **unexposed portion** with a second mask pattern to thereby repair the pattern transferred by the defective photomask (see Abstract; Figure 2A-2F; column 2, line 65, column 2, line 18, column 2, lines 60-67; claims 1 and 10).

The Applicants respectfully submit that Higashikawa et al does not disclose or suggest Applicants invention including:

> "exposing a semiconductor wafer to a **first mask part** that is **at least partially defective** to form a defectively exposed portion; and,
>
> **exposing the defectively exposed portion** to a second mask part corresponding to the first mask part and that is at least **substantially free from defects** or **with defects at different locations**"

As such, the Applicants respectfully submit that Higashikawa et al is insufficient to make out a *prima facie* case of anticipation with respect to Applicants disclosed and claimed invention.

It is well recognized that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The rejection of Claims 25-30,32,33 and 39 under 35 USC §

102(b) based on Higashikawa et al is respectfully traversed. A reconsideration for allowance of Claims 25-30,32,33 and 39 is respectfully requested of the Examiner.

Based on the foregoing, Applicants respectfully submit that all the pending claims, i.e. Claims 25-30,32,33 and 39 are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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